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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :   Before the Examiner:
     I. Holland, et al.   :   J. Mills

Serial No.: 08/890,643   :   Group Art Unit: 2171

Filed: July 9, 1997

                        :   IBM Corp.

Title: SIMULATION OF   :   Intellectual Property Law
        MEMORY-MAPPED I/O   :   11400 Burnet Road
                        :   Austin, Texas 78758

REPLY BRIEF

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

In response to the Examiner's Answer having a mailing date of December 19, 2000 (Paper No. 14), with a one-month shortened statutory period for response set to expire on January 19, 2001, Appellants hereby respond to arguments made by the Examiner in the Examiner's Answer.
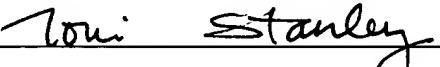
The Examiner disputes the accuracy of Appellants' Summary of Invention in Section V of Appellants' Appeal Brief (Paper No. 13). The Examiner further asserts that Appellants' Summary of Invention is beyond the scope of the claims and appears to elaborate on features of the Specification which are not directly at issue in this case. In response, Appellants respectfully traverse this assertion by the Examiner in that Appellants' Summary of Invention in Section V of the Appeal Brief elaborates on features recited within claims other than claim 1.

With respect to the Examiner's Arguments on pages 3-6 of Paper No. 14, Appellants respectfully assert that the Examiner has added new grounds of rejection, since the Examiner has asserted new arguments not made beforehand in any of the previous office actions; therefore, Appellants are hereby permitted to respond to such new arguments.

On page 4 of the Examiner's Answer, the Examiner has stated:

> The applicant argues that a shared library is a collection of routines, but as set forth in the office action, shared memory may also be a collection of routines or data or other structures which may be shared by the processor.

This is a new argument by the Examiner, never before stated by the Examiner in any previous office actions. In all previous office actions, the Examiner has merely stated that "the shared memory is taught by the reference as the shared memory segments taught on Col 16, line 21." Moreover, never before has the Examiner stated that "shared memory may also be a collection of routines or data or other structures which may be shared by the processor," which contradicts the Examiner's assertion that he has set forth this statement in a previous office action. Yet still further, even if the Examiner is merely parroting Appellants' arguments on page 6 of the Appeal Brief, the Examiner is misquoting Appellants, since Appellants did not add to this statement the words "or data or other structures which may be shared by the processor." And, still further, *Blackard*

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does not teach that a shared memory may also be a collection of routines or data or other structures which may be shared by the processor.

Therefore, the Examiner has failed to prove a *prima facie* case of anticipation in rejecting claims 4, 10 and 16, since the Examiner has failed to prove that *Blackard* teaches the limitations specifically recited within these claims.

With respect to claim 5, Appellants respectfully assert that the Examiner has added new arguments in the Examiner's Answer. In all previous office actions, all the Examiner has stated with respect to claim 5 is that "the read only file being a data base file is inherent in the teaching of the reference and that the data in the read only file may be formatted [sic] as a database." Now, in the Examiner's Answer, the Examiner has further argued:

> The prior art reference shows that the read only file is copied from ROM and as broadly claimed by the applicant without anything in addition, it is well known that file may be characterized as a database or other data structure. The applicant asserts that BIOS is not a database but the applicant's claim as broadly read does not attach any patentable significance to the word database that would prevent a BIOS from being a database structure.

Appellants respectfully traverse these assertions by the Examiner. Appellants respectfully remind the Examiner that it is his burden to prove a *prima facie* case of anticipation that each and every element recited within the claim is found within the cited prior art reference. Instead, what the Examiner is attempting to do is to state that a BIOS may be a database file, and follows that with an assertion that Appellants must disprove this statement. The Examiner is relying upon what he considers to be his broad interpretation of the limitations within the claim. The problem with the Examiner's line of argument is that he is applying an unreasonable definition of BIOS when he claims that a BIOS may be the same as a database file. A BIOS is not an indefinite thing, but is well known in the art as a basic input/output system set of routines that work closely with the

hardware to support the transfer of information between elements of the system, such as memory, disk, and the monitor. See definition of BIOS, Microsoft Press Computer Dictionary, page 37, copyright 1999 by Microsoft Press. There is no need for Appellants to further define within the claims what a BIOS is, in contrast to the Examiner's assertion. In fact, Appellants respectfully assert that it is well known in the art that a BIOS is not a database file, and that this adequately rebuts the Examiner's *prima facie* case of anticipation in rejecting claim 5, and it is therefore the Examiner's burden to prove that a BIOS can be the same as a database file with <u>objective</u> evidence.

As a result of the foregoing, Applicants respectfully assert that the Examiner has still failed to prove a *prima facie* case of anticipation in rejecting claims 5, 11 and 17.

With respect to claim 6, Appellants respectfully assert that the Examiner has presented a new argument on page 5 of the Examiner's Answer, when the Examiner asserts that "the prior art reference teaches instruction address translation on Col 13, line 22, *et seq.* which performs essentially the same function as making the read only code into executable code." In all previous office actions the Examiner has merely asserted that "the wrapping of the read only file with executable code is inherent in the reference teaching of the instruction address translation." In response to this new argument by the Examiner, Appellants respectfully assert that on pages 7 and 8 of the Appeal Brief, Appellants have adequately asserted that the step of wrapping the read-only file with executable code is not the same function as the instruction address translation discussed in *Blackard*. Therefore, Appellants respectfully assert that it the Examiner's burden to now respond to Appellants' assertions in the Appeal Brief as is required under MPEP § 707.07(f). As a result of the foregoing, Appellants respectfully assert that the Examiner has still failed to prove a *prima facie* case of anticipation in rejecting claims 6, 12 and 18.

With respect to claims 19 and 20, Appellants respectfully assert that the Examiner has added in a new argument by asserting "that the type of data stored whether image or

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audio which does not add anything to the function or structure of the invention is not a patentable distinction." In response, Appellants respectfully assert that when a limitation is present within a claim, it is the Examiner's burden to address each and every limitation in a Section 102 rejection, and the Examiner may not merely ignore a limitation as the Examiner is doing in this case by stating that such limitations do not add anything to the function or structure of the invention. The only reason the Examiner is making this statement is that the Examiner knows that he cannot meet his burden under Section 102 of showing that these limitations are taught within *Blackard*.

With respect to claims 21-23, Appellants assert in a similar vein as above with respect to claims 19 and 20, that the Examiner cannot ignore the specific recitations within these claims by merely asserting that "adding headers which are well known in the art and not significant in the design and operation of the invention." In fact, the significance of these limitations can be found within Appellants' Summary of Invention on page 3 of the Appeal Brief where Appellants state that the code converter 302 "is a tool that wrappers the read-only data with code headers and records in order to make the operating system loader 202 believe that the read-only file is executable code." Therefore, Appellants respectfully assert that the Examiner has failed to prove a *prima facie* case of anticipation in rejecting claims 21-23.

With respect to claims 24-26, Appellants again respectfully assert that the Examiner is adding in new arguments on pages 5-6 of the Examiner's Answer, and Appellants respectfully traverse these assertions by the Examiner. The Examiner is misquoting the Abstract of *Blackard* by asserting that the abstract teaches that the simulator takes additional steps to guarantee the correct execution of modified instructions thus protecting the processor. Nowhere is it stated that the simulator performs these additional steps to protect the processor. This has nothing to do with a processor operating in a protected mode. Appellants note that an Examiner may take a broad interpretation of claims, but the Examiner must still correctly cite teachings within

a prior art reference. In this case, the Examiner has misquoted the prior art reference in

his rejection.

In conclusion, Appellants respectfully assert that all of the claims in the

application are patentable over *Blackard*.

Respectfully submitted,
WINSTEAD SECHREST & MINICK P.C.
Attorneys for Applicant
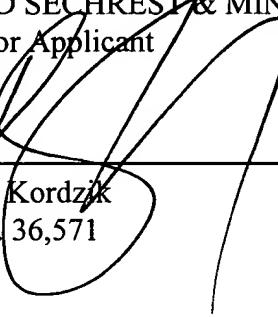
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